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MILITARY STANDARD

AIRCRAFT INTERNAL TIME DIVISION COMMAND/RESPONSE MULTIPLEX DATA BUS

FSC MISC

DEPARTMENT OF THE AIR FORCE

Washington D. C. 20330

MIL-STD-1553A(USAF)

Aircraft Internal Time Division Command/Response Multiplex Data Bus

1. This Military standard has been approved for use by all Departments and Agencies of the Department of Defense.

2. Recommended corrections, additions, or deletions should be addressed to Aeronautical Systems Division, ATTN: ENYESS, Wright-Patterson Air Force Base, Ohio 45433.

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1. SCOPE AND PURPOSE

1.1 Scope. This standard defines requirements for digital, command/response, time division multiplexing (Data Bus) techniques on aircraft. It encompasses the data bus line and its interface electronics as illustrated on figure 1, and also defines the concept of operation and information flow on the multiplex data bus and the electrical and functional formats to be employed.

1.2 Purpose. The purpose of this document is to establish uniform requirements for multiplex data system techniques which will be utilized in systems integration of aircraft subsystems and to promote standard digital interfaces for associated subsystems. The system designer retains the flexibility to assemble a custom multiplex system from the functionally standard parts and to program the standard electronic functions in order to provide a control mechanism, traffic patterns, redundancy, and a viable degradation concept.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bid or request for proposal, form a part of the standard to the extent specified herein.

SPECIFICATION

Military

MIL-E-6051 Electromagnetic Compatibility Requirements, Systems

STANDARDS

Military

MIL-STD-461 Electromagnetic Interference Characteristics, Requirements for Equipment
MIL-STD-462 Electromagnetic Intereference Characteristics, Measurement of

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

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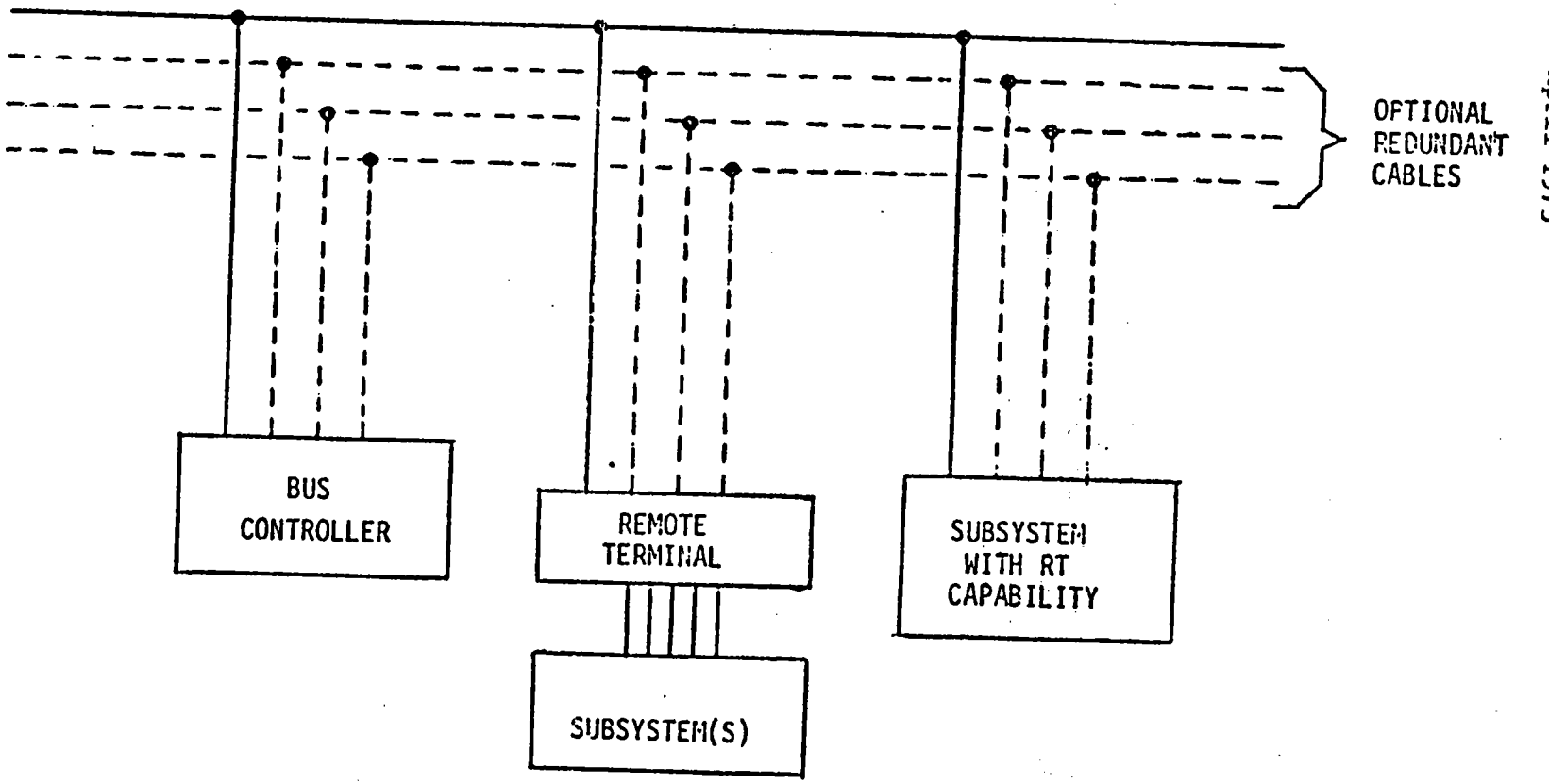


Figure 1. Typical Multiplex Data Bus Architecture

3. DEFINITIONS

3.1 Remote terminal. The remote terminal is the electronics necessary to interface the bus with the subsystem and the subsystem with the bus. This electronics may exist as a separate LRU (line replaceable unit), or be contained within the users' subsystem. A redundant bus controller, when not functioning as a controller, may operate as a remote terminal.

3.2 Bit. Contraction of binary digit: may be either zero or one. In information theory a binary digit is equal to one binary decision or the designation of one of two possible values or states of anything used to store or convey information.

3.3 Bit rate. The number of bits transmitted per second.

3.4 Pulse code modulation (PCM). The form of modulation in which the modulation signal is sampled, quantized, and coded so that each element of information consists of different types or numbers of pulses and spaces.

3.5 Time division multiplexing (TDM). The transmission of information from several signal channels through one communication system with different channel samples staggered in time to form a composite pulse train.

3.6 Command/response mode. The operation of a bus system in which the remote terminal will respond only when commanded by the bus controller.

3.7 Half duplex. Operation of a data transfer system in either direction over a single line, but not in both directions on that line simultaneously.

3.8 Asynchronous operation. For the purpose of this standard, asynchronous bus operation implies an independent clock source at each remote terminal which is utilized for the transmission of messages. The received message shall be decoded using clock information derived from the received signal.

3.9 Dynamic bus allocation. The operation of a bus system in which designated remote terminals are offered control of the data bus.

3.10 Word. In this document a word is a sequence of 16 bits plus sync and parity. There are three types of words: command, status and data.

3.11 Message. A message is a transmission of words on the data bus cable. A message transfer is complete when the command word, data word(s), and the status word have been transmitted. There are three types of messages: controller to terminal, terminal to controller and terminal to terminal.

3.12 Data bus. Whenever a data bus or bus is referred to in this document it shall imply a single twisted shielded pair cable.

3.13 Controller. The controller shall be a unit that is either programmable, or controlled by a processor, and that serves the function of commanding, scanning and monitoring bus traffic.

4. REQUIREMENTS

4.1 Data bus operation. The multiplex data bus in its most elemental configuration shall operate as shown on figure 1. The data bus shall function asynchronously in a command/response mode, and transmission shall occur in a half-duplex manner. Sole control of information transmission on the bus shall reside with the bus controller, which shall initiate all transmissions. The information flow on the data bus shall be comprised of messages which are, in turn, formed by three types of words (command, data, and status) as defined in 4.2.3.5. All elements of the data bus, including the transmission line, remote terminal and controller, shall conform to the electromagnetic interference requirements specified in MIL-STD-461 and the electromagnetic compatibility requirements of MIL-E-6051.

4.1.1 Information transfer modes. The data bus may employ three modes of information transfer: (1) bus controller to remote terminal (RT) transfer, (2) RT to controller transfer, and (3) RT to RT transfer. These modes shall operate as described in 4.2.3.6 and subparagraphs.

4.2 Characteristics.

4.2.1 Data form. Digital data may be transmitted in any desired form, provided that the chosen form shall be compatible with the message and word formats defined in this standard. Any unused bit positions in a word shall be transmitted as logic zeros.

4.2.2 Bit priority. The most significant bit shall be transmitted first with the less significant bits following in descending order of value. The number of bits required to define a quantity shall be consistent with the resolution or accuracy required. In the event double precision quantities (information accuracy or resolution requiring more than 16 bits) are transmitted, the more significant half shall be transmitted first, followed by the less significant half.

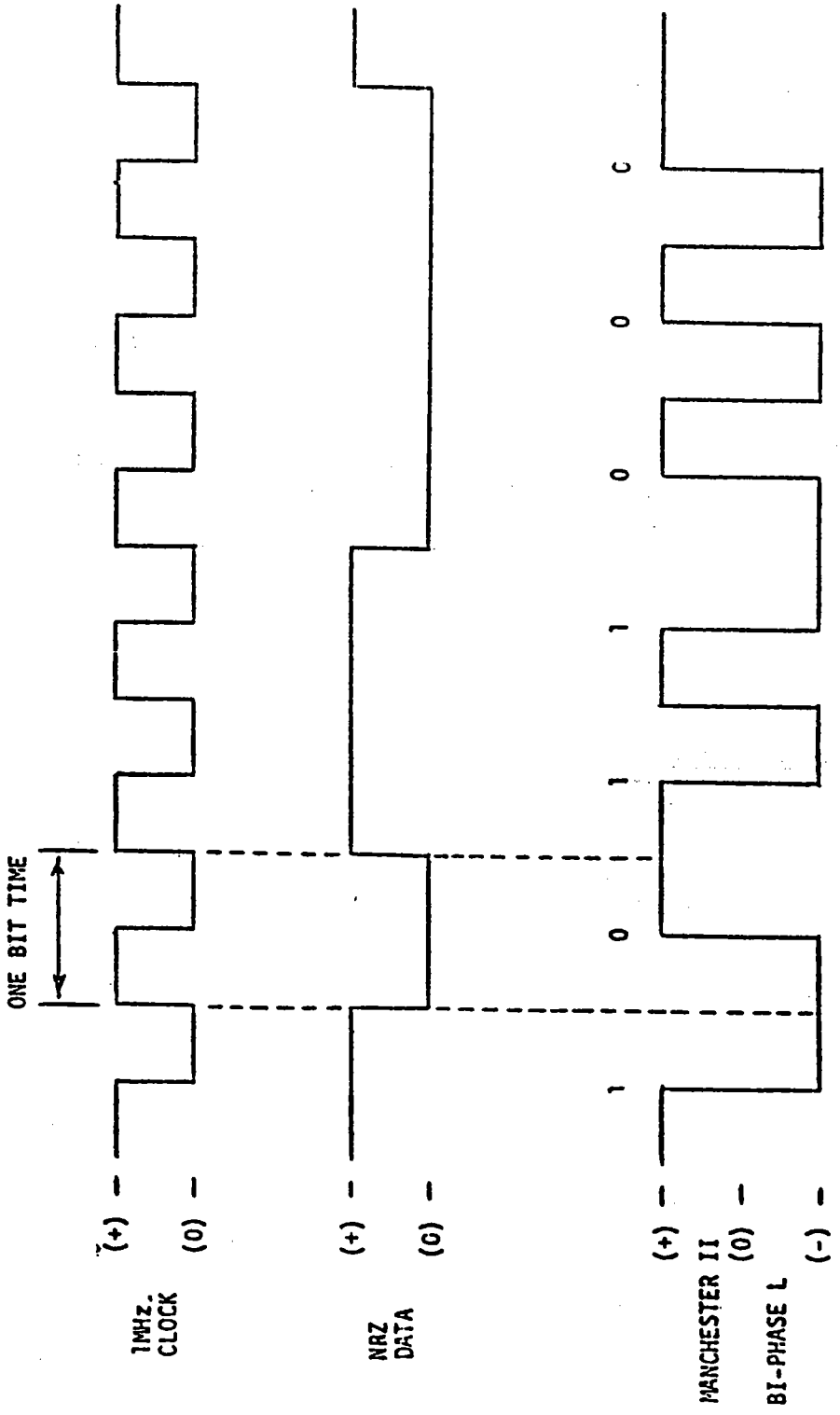


Figure 2. Data Encoding

4.2.3 Transmission method.

4.2.3.1 Modulation. The signal shall be transferred over the data bus in serial digital pulse code modulation form.

4.2.3.2 Data code. The data code shall be Manchester bi-phase level. A logic one shall be transmitted as a bipolar coded signal 1/0 (i.e., a positive pulse followed by a negative pulse). A logic zero shall be bipolar coded signal 0/1 (i.e., a negative pulse followed by a positive pulse). A transition through zero occurs at the midpoint of each bit time (see figure 2).

4.2.3.3 Transmission rate. The transmission rate on the bus shall be 1.0 megabit per second with a long term stability of $\pm$0.01 percent (i.e., $\pm$100 Hz). The short term stability (i.e., stability over a 1.0 second interval) shall be at least 0.001 percent (i.e., $\pm$10 Hz).

4.2.3.4 Word size. The word size shall be 16 bits plus the sync waveform and the parity bit for a total of 20 bit times as shown in figure 3.

4.2.3.5 Word formats. The word formats shall be as shown on figure 3 for the command, data, and status words.

4.2.3.5.1 Command word. A command word shall be comprised of a sync waveform, address, transmit/receive bit, subaddress/mode, data word count, and a parity bit (see figure 3), except as modified by 4.2.3.5.1.7.

4.2.3.5.1.1 Sync. The command sync waveform shall be an invalid Manchester waveform as shown on figure 4. The width shall be three bit times, with the waveform being positive for the first one and one-half bit times, and then negative for the following one and one-half bit times. If the next bit following the sync is a logic zero, then the last half of the sync waveform will have an apparent width of two clock periods due to the Manchester encoding.

4.2.3.5.1.2 Address. The next five bits following the sync shall be the RT address. This permits a maximum of 32 RTs to be attached to any one data bus. All 1's shall indicate a decimal address of 31, and all 0's shall indicate a decimal address of 32. The most significant bit of the address shall be transmitted first.

4.2.3.5.1.3 Transmit/receive. The next bit following the address shall be the transmit/receive bit, which shall indicate the action required of the RT. A logic zero shall indicate the RT is to receive, and a logic one shall indicate the RT is to transmit.

4.2.3.5.1.4 Subaddress/mode. The next five bits following the transmit/receive bit shall be utilized for either a RT subaddress or mode control, as is dictated by the individual terminal requirements. The subaddress/mode value of 00000 is reserved for special purposes, as specified in 4.2.3.5.1.7, and shall not be utilized for any other function.

4.2.3.5.1.5 Word count. The next five bits following the subaddress/mode control shall be the quantity of data words to be either sent out or received by the RT. A maximum of 32 data words may be transmitted or received in any one message block. All 1's shall indicate a decimal count of 31, and all 0's shall indicate a decimal count of 32.

4.2.3.5.1.6 Parity. The last bit in the word shall be used for parity over the preceding sixteen bits. Odd parity shall be utilized.

4.2.3.5.1.7 Optional mode control. For RTs exercising this option, a subaddress/mode code of 00000 shall imply that the contents of the word count field are to be decoded as a five bit mode command. When used with this option, the word count field mode code of 00000 shall be reserved for dynamic bus allocation.

4.2.3.5.2 Data word. A data word shall be comprised of a sync waveform, data bits, and a parity bit (see figure 3).

4.2.3.5.2.1 Sync. The data sync waveform shall be an invalid Manchester waveform as shown on figure 5. The width shall be three bit times, with the waveform being negative for the first one and one-half bit times, and then positive for the following one and one-half bit times. Note that if the bits preceding and following the sync are logic ones, then the apparent width of the sync waveform will be increased to four bit times.

4.2.3.5.2.2 Data. The sixteen bits following the sync shall be utilized for data transmission as specified in 4.2.2.

4.2.3.5.2.3 Parity. The last bit shall be utilized for parity as specified in 4.2.3.5.1.6.

4.2.3.5.3 Status word. A status word shall be comprised of a sync waveform, RT address, message error bit, status codes, terminal flag bit, and a parity bit (see figure 3).

4.2.3.5.3.1 Sync. The sync waveform shall be as specified in 4.2.3.5.1.1.

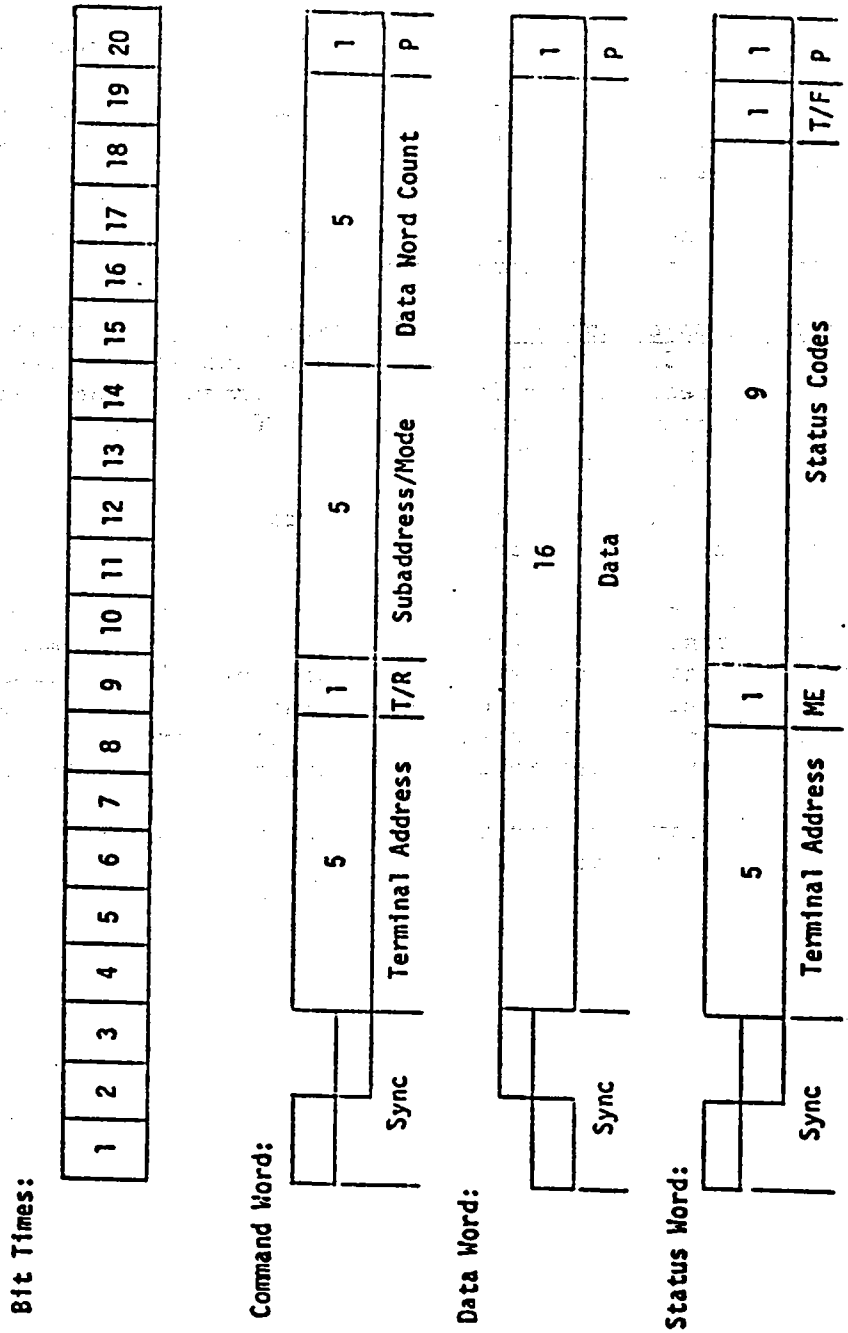
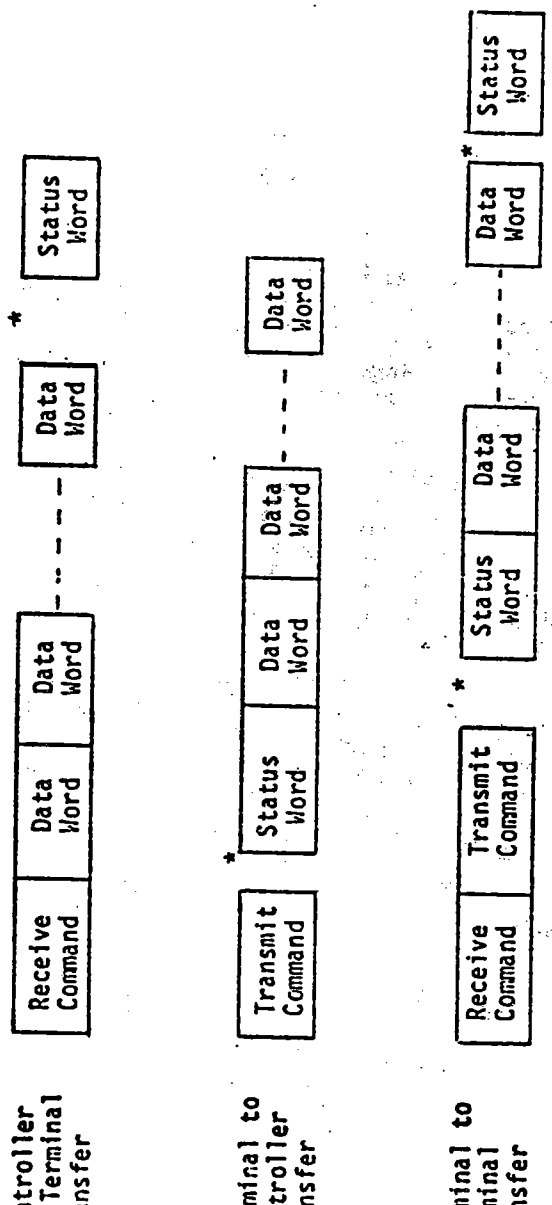


Figure 3. Word Formats



* Gap as specified in 4.3.1

Figure 6. Message Formats

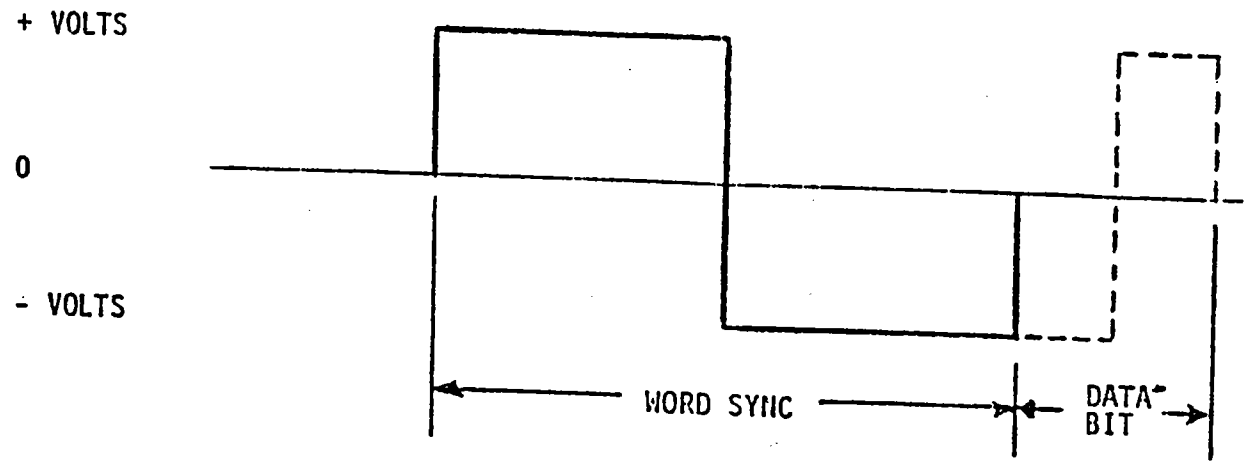


Figure 4. Command and Status Sync

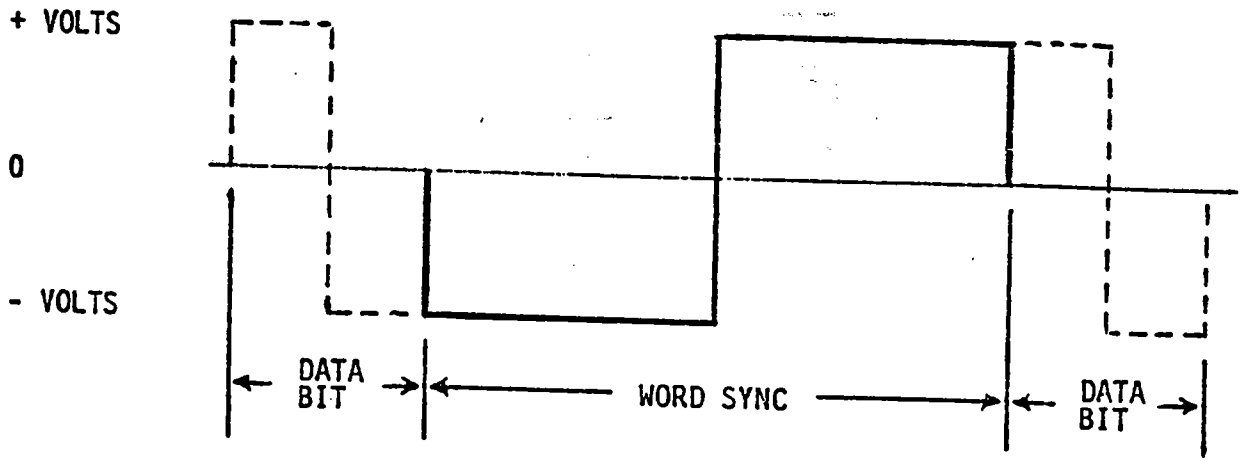


Figure 5. Data Sync

4.2.4 Transmission line. The data bus shall utilize, as the transmission medium, a twisted, shielded, wire pair.

4.2.4.1 Cable. The cable used shall be a two conductor, twisted, shielded, jacketed cable. The wire-to-wire distributed capacitance shall not exceed 30.0 picofarads per foot. The cable shall be formed with not less than one twist per inch; and the cable shield shall provide a minimum of 80 percent coverage.

4.2.4.2 Characteristic impedance. The characteristic impedance shall be 70 ohms, plus or minus 10 percent, at a sinusoidal frequency of 1.0 MHz.

4.2.4.3 Cable attentuation. At the frequency of 4.2.4.2, the cable power loss shall be 1 db/100 ft or less.

4.2.4.4 Cable length. The cable length of any main bus may be up to 300 feet.

4.2.4.5 Cable termination. The cable shall be coupled to the RT as shown on figure 7. A long stub is defined as any stub greater than one foot in length. The use of long stubs is discouraged and the length of any stub shall not exceed 20 feet. The two ends of the cable shall be terminated with a resistance equal to the cable characteristic impedance.

4.2.4.6 Cable coupling. All connections to the data bus shall utilize a small shielded coupler box. This box shall be of sufficient size to permit the installation of the transformer and isolation resistors specified in 4.2.5. The connector plug shall be compatible with Amphenol Type 31-235 or Trompeter Type TEI-14949-EI37 receptacles. The connector receptacle shall be compatible with Amphenol type 31-224 or Trompeter Type TEI-14949-PL36 plugs. The polarity convention shall be that the female connection in the plug is positive, and the male connection in the receptacle is positive. This connector, with the indicated polarities, shall be used for all bus interfaces.

4.2.4.7 Wiring and cabling for EMC. For purposes of electromagnetic compatibility (EMC), the wiring and cabling provisions of MIL-E-6051 shall apply.

4.2.5 RT/bus interface circuits.

4.2.5.1 Circuit configuration. The input/output circuits shall consist of a transmitter-receiver, DC isolation/coupling transformer, and isolation resistors as configured on figure 7.

4.2.3.5.3.2 RT address. The next five bits following the sync shall contain the address of the terminal which is transmitting the status word as defined in 4.2.3.5.1.2.

4.2.3.5.3.3 Message error. The first bit after the address shall be utilized to indicate that the preceding message failed to pass the RT's validity tests. This error condition shall include parity errors. A logic one shall indicate the presence of a message error, and a logic zero its absence. A message error shall be indicated when the preceding message to a RT has failed either the word or message validity criteria for the RT. The criteria shall include those specified in 4.2.5.4.4.

4.2.3.5.3.4 Status codes. The next nine bits following the message error bit may be utilized in any fashion desired by the RT designer, except that all zeros shall indicate a normally functioning terminal.

4.2.3.5.3.5 Terminal flag. The next to least significant bit in the status word is reserved for a terminal flag bit. This bit shall be set to one to indicate the need for the bus controller to examine the built in test data available from the terminal.

4.2.3.5.3.6 Parity. The last bit shall be utilized for parity as specified in 4.2.3.5.1.6.

4.2.3.6 Message formats. The messages transmitted on the data bus shall be in accordance with the formats in figure 6. The maximum and minimum response times shall be as stated in 4.3.1.

4.2.3.6.1 Controller to RT transfers. The controller shall issue a receive command followed by the specified number of data words. The RT shall, after message validation, transmit a status word back to the controller. The command and data words shall be transmitted in a continuous fashion with no interword gaps.

4.2.3.6.2 RT to controller transfers. The controller shall issue a transmit command to the RT. The RT shall, after command verification, transmit a status word back to the controller, followed by the specified number of data words. The status and data words shall be transmitted in a continuous fashion with no interword gaps.

4.2.3.6.3 RT to RT transfers. The controller shall issue a receive command to RT A, followed by a transmit command to RT B. RT B shall then transmit the data as specified in 4.2.3.6.1.

4.2.5.2 Fault isolation. An isolation resistor shall be placed in series with each connection to the data bus cable. This resistor shall have a value of 0.75 Z_o ohms plus or minus 5 percent where Z_o is the cable characteristic impedance. The impedance placed across the data bus cable shall be no less than 1.5 Z_o ohms for any failure of the coupling transformer, cable stub, or RT transmitter/receiver.

4.2.5.3 RT output characteristics.

4.2.5.3.1 Output levels. The RT signal output circuitry shall be capable of driving the cable specified in 4.2.4.1 and not less than 33 other RTs, as specified herein, each attached to the cable by means of a cable stub of maximum length specified in 4.2.4.5. The output circuitry shall maintain the specified operation with the exception of a 25 percent maximum reduction of the data bus signal amplitude in the event that one of the RTs has a fault that causes it to reflect the fault impedance specified in 4.2.5.2 on the bus. The RT peak signal output voltage shall be between plus or minus 3.0 and 10.0 volts, line-to-line, when measured at the data bus cable connection (point A on figure 7).

4.2.5.3.2 Output waveform. The waveform when observed at point C in figure 7 shall have zero crossings which deviate not more than plus or minus 25 nanoseconds from those shown in figure 8. The rise and fall time of this waveform shall be equal to or greater than 100 nanoseconds when measured from levels of 10 to 90 percent of full waveform peak-to-peak, voltage as shown in figure 8.

4.2.5.3.3 Output noise. Any noise transmitted to the data bus when the RT is receiving or has power removed, shall not exceed a value of 10.0 millivolts peak-to-peak, line-to-line, as measured at the point specified in 4.2.5.3.1.

4.2.5.4 RT input characteristics.

4.2.5.4.1 Input waveform compatibility. The RT shall be capable of receiving and operating with the incoming signals specified herein, and shall accept waveforms varying from a square wave to a sine wave. The RT shall respond to an input signal whose positive or negative peak amplitude, line-to-line, is within the range of 10.0 to 0.5 volts. The voltages are measured at point C in figure 7.

4.2.5.4.2 Common mode rejections. Any signals from dc to 2.0 MHz, with amplitudes equal to or less than plus or minus 10.0 volts peak, line-to-ground, applied to point A as shown in figure 7 shall not degrade the performance of the RT.

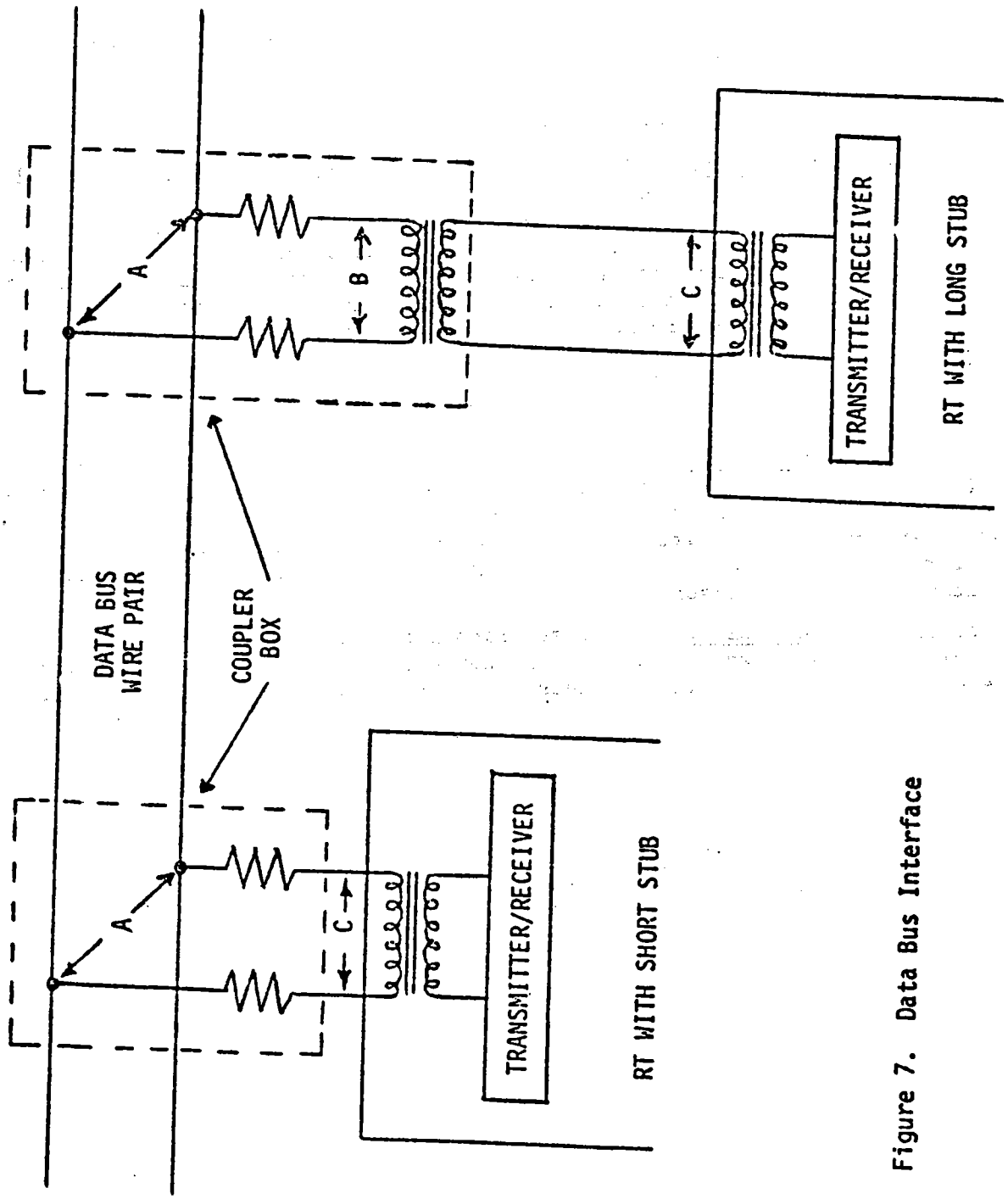


Figure 7. Data Bus Interface

4.2.5.4.3 Input impedance. The magnitude of the RT input impedance, when the RT is not transmitting, or has power removed, shall be a minimum of 2000 ohms within the frequency range of 100 KHz to 1.0 MHz. This impendance is that measured line-to-line at point C on figure 7.

4.2.5.4.4 Data validation. Logic shall be provided in each RT to recognize improperly coded signals, data dropouts, or excessively noisy signals. Each word shall conform to the following minimum validating criteria:

a. The word begins with a valid sync field

b. The bits are in a valid Manchester II code

c. The information field has 16 bits plus parity

d. The word parity is odd.

Where a word fails to conform to the preceding criteria, the word shall be considered invalid and shall not be used by the receiving RT. Where an invalid word sync occurs, the receiving RT shall reset and wait for a new valid message sync. An invalid word count shall be construed as a message transmission error.

4.3 Terminal operation. The remote terminal shall operate in response to commands received from the bus controller. The RT shall be capable of receiving a command word at any time except when it is transmitting. A second command word sent to a terminal after it is already operating on one shall invalidate the first command and cause the RT to begin operation on the second command.

4.3.1 Response time. The RT shall respond to a valid transmit data command during the time period 2.0 to 5.0 microseconds after receipt of the last bit of the command word. The RT shall respond to a valid receive data command during the time period 2.0 to 5.0 microseconds after receipt of the last bit of the last data word.

4.3.2 Terminal fail-safe operation. The RT shall contain the self-test circuitry necessary to detect an erroneous transmission of data on to the data bus. This circuitry shall include a transmission time-out which will preclude a signal transmission period of greater than 660 microseconds (one status, and thirty-two data words). When the self-test circuitry detects any such erroneous transmission, it shall automatically shut down the transmitter portion of the RT.

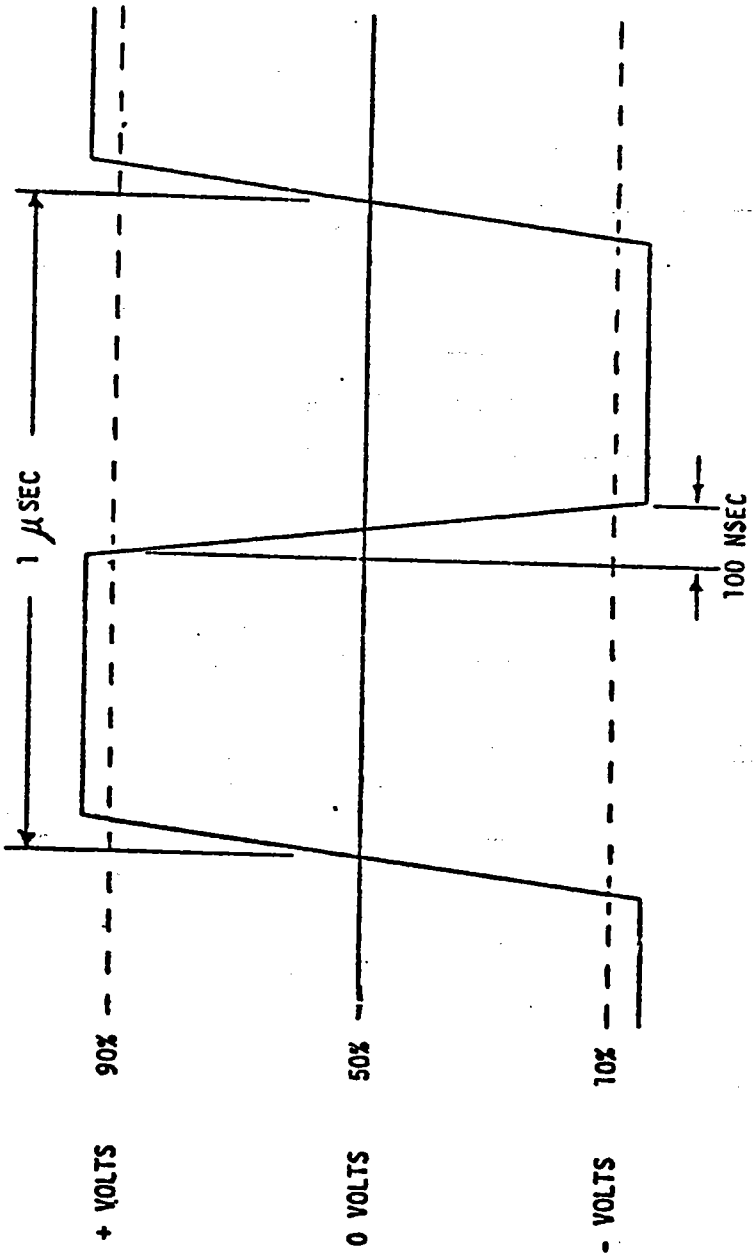


Figure 8. Output Waveform

4.3.3.4 Test conditions. For purposes of the noise tests, the following conditions shall be observed. All data words shall be changed to random bit patterns prior to each transmission/reception set as defined in 4.3.3.2. The test shall be conducted with the bus controller and the remote terminal both connected by 20 foot stubs to the main data bus cable, with a minimum distance of 100 feet between the stubs. The remote terminal transmitter shall provide an output as specified in 4.2.5.3. The bus controller transmitter shall have its output adjusted so as to provide the minimum signal amplitude specified in 4.2.5.4.1 at the remote terminal.

4.4 Terminal to subsystem interface. For those applications where a terminal is not contained within a subsystem, and the terminal exists as a distinct LRU, the terminal shall provide the necessary electronics to interface to the subsystem. The terminal shall have provisions for the standard serial digital and discrete interfaces as defined in the following paragraphs. All other signals shall require special purpose interface provisions within the terminal, this electronics being designed for the peculiar interface requirement.

4.4.1 Serial digital interface. The standard serial digital interface shall be configured as shown in figure 9. All lines are unidirectional, with the data line's direction to be determined by its usage, i.e., to transmit or to receive data. The interface shall operate as defined in 4.4.1.1 for an input interface and as defined in 4.4.1.2 for an output interface. The functions of each of the signals is as defined in table I.

4.4.1.1 Serial digital input. A serial digital input interface is a set of six signals between an external device and the remote terminal. This interface is shown in figure 10. The function of each of the six signals is defined in table I. The performance of a data input sequence can be initiated by either of two actions. The external device can pulse the FLAG line if the LOCKOUT line is low, and thereby initiate a data input sequence. The timing diagram for this action is shown in figure 11. The bus controller can directly command the remote terminal to begin a data input sequence. The timing diagram for this action is shown in figure 12. In either case, the initiation of the data input sequence causes the LOCKOUT line to be set, and the completion of the data input sequence shall cause the remote terminal to notify the bus controller of the data input, and of any parity errors. The remote terminal shall be required to clear the LOCKOUT before any new externally initiated data input sequences can occur.

4.3.3 Noise environment operation. The remote terminal shall function properly under the test conditions specified in 4.3.3.4, and encountering the electromagnetic environment specified in 4.3.3.1. The remote terminal shall exhibit a maximum bit error rate of 10^{-12}, where the bit error rate is as defined in 4.3.3.2. The remote terminal shall also exhibit a maximum incomplete message rate of 10^{-6}, where the incomplete message rate is as defined in 4.3.3.3.

4.3.3.1. Test environment. The test environment for the remote terminal and data bus cable radiated susceptibility shall be as follows:

4.3.3.1.1 Electric field. The electric field test shall employ MIL-STD-462 method RS03, with the limit specified in MIL-STD-461 test limit RS03. The electric field shall be 100 percent modulated by a waveform as specified in 4.2.3.

4.3.3.1.2 Magnetic field. The magnetic field (spike test) shall employ MIL-STD-462 method RS02, with the limit specified in MIL-STD-461 test limit RS02.

4.3.3.2 Bit error rate. For the purposes of paragraph 4.3.3, the bit error rate is defined as follows: The bus controller transmits 32 data words to a remote terminal as specified in 4.1, and the remote terminal responds with a status word indicating no message errors. The bus controller then commands the remote terminal to transmit the same 32 data words which it previously received, as is specifed in 4.1. Upon receipt of a valid response from the remote terminal, the controller than compares each data word which it sent to the remote terminal with each one it received back from the remote terminal. The sixteen bits in each word pair are compared and if any bit does not match, this is to be considered a bit error. The total number of data bits transmitted during a specific time period are counted. The bit error rate is then defined as the number of bit errors, divided by the total number of bits transmitted.

4.3.3.3 Incomplete message rate. For the purposes of paragraph 4.3.3, the incomplete message rate is defined as follows: A message is the set of command, data, and status words as defined in 4.2.3.6. An incomplete message is defined as one during which the remote terminal does not properly respond to a command by the bus controller, or one in which the message error bit is set in the remote terminal status word. The total number of incomplete messages are counted during a specific time period, as are the total number of messages. The incomplete message rate is given by the number of incomplete messages divided by the total number of messages. The message error bit in the first status word following a non-response by a remote terminal shall not be included in the incomplete message count. The message formats shall be as defined in 4.3.3.2.

TABLE I

Signal Definitions for Serial Digital Interfaces

1. REQUEST. This is a signal from the remote terminal to the external device which, when set to logic 1 by the remote terminal, notifies the external device that a data transfer is about to take place, and when set to logic Ø by the remote terminal, notifies the external device that a data transfer is complete.

2. ACKNOWLEDGE. This is a signal from the external device to the remote terminal which, when set to logic 1 by the external device, notifies the remote terminal that the external device has recognized the REQUEST, and is ready for the data transfer, and when set to logic Ø by the external device, notifies the remote terminal that the external device has recognized the lowering of the REQUEST and the end of the data transfer.

3. CLOCK. This is a signal from the remote terminal to the external device, which when active is a 1 MHz square wave, with a number of cycles equal to the number of bits to be shifted. The CLOCK is not started until the remote terminal has seen the ACKNOWLEDGE line raise. At the end of the last CLOCK cycle the remote terminal shall lower the REQUEST Line.

4. DATA. This is a signal to or from the remote terminal upon which data is transmitted. On the positive edge of the CLOCK signal the next DATA bit shall be placed on the DATA line.

5. LOCKOUT. This is a signal from the remote terminal to the external device which, when set to logic 1 by the remote terminal, notifies the external device that it shall refuse all external requests for data transfer, and when set to logic Ø by the remote terminal, notifies the external device that it shall allow external requests for data transfer.

6. ERROR. This is a signal from the external device to the remote terminal which the external device clears at the time ACKNOWLEDGE is raised, and which the external device sets at any time that a parity error is detected while receiving data.

7. FLAG. This is a signal from the external device to the remote terminal, which is a pulse of duration between 1 and 10 microseconds, that notifies the remote terminal that there has been an external request for a DATA input sequence. The occurrence of this pulse shall initiate a DATA input sequence, and after the sequence is completed the bus controller shall be informed that the sequence occurred and whether or not there were any parity errors. This signal cannot occur while the LOCKOUT line is high, and the occurrence of this signal causes the LOCKOUT line to be set high.

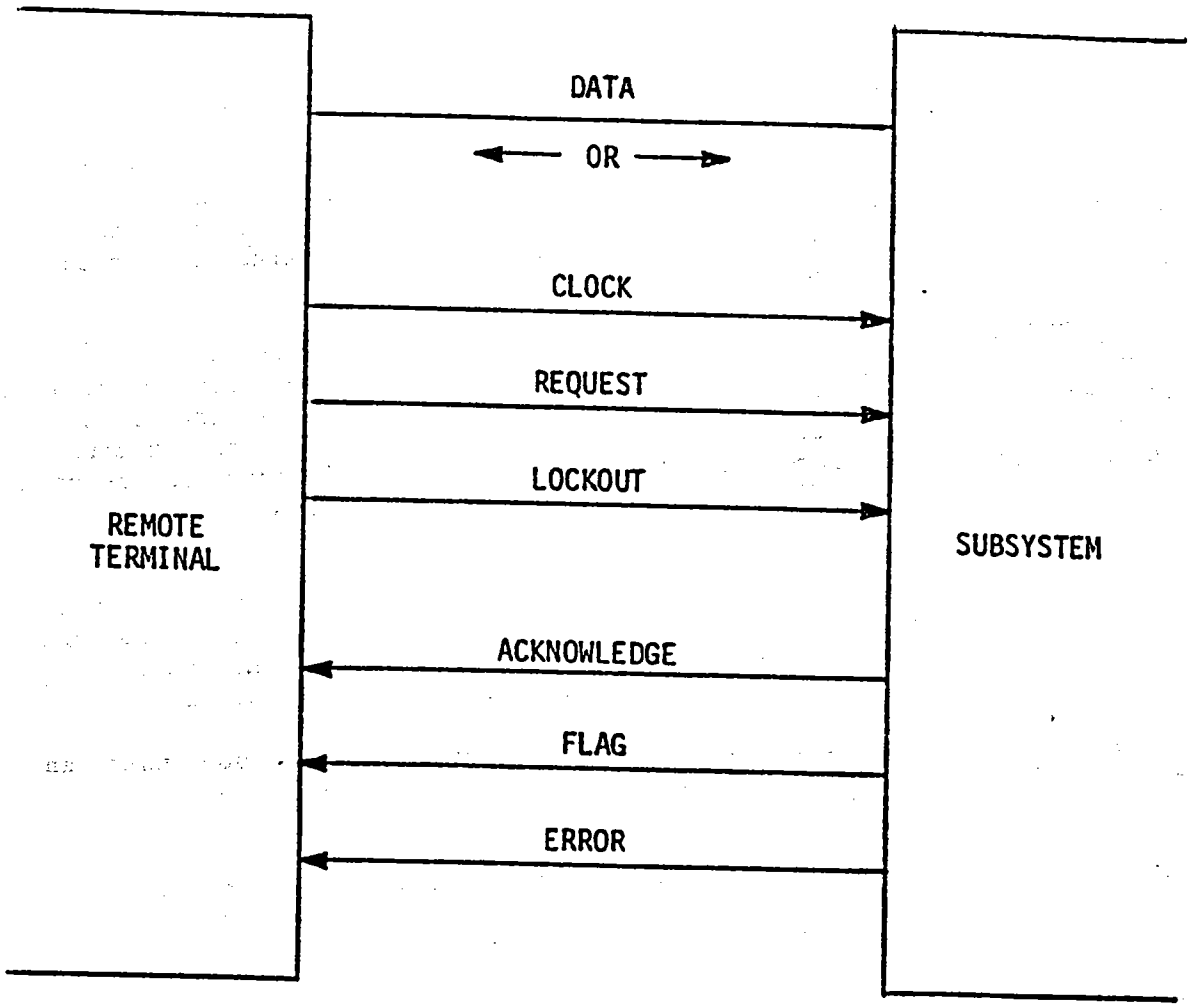
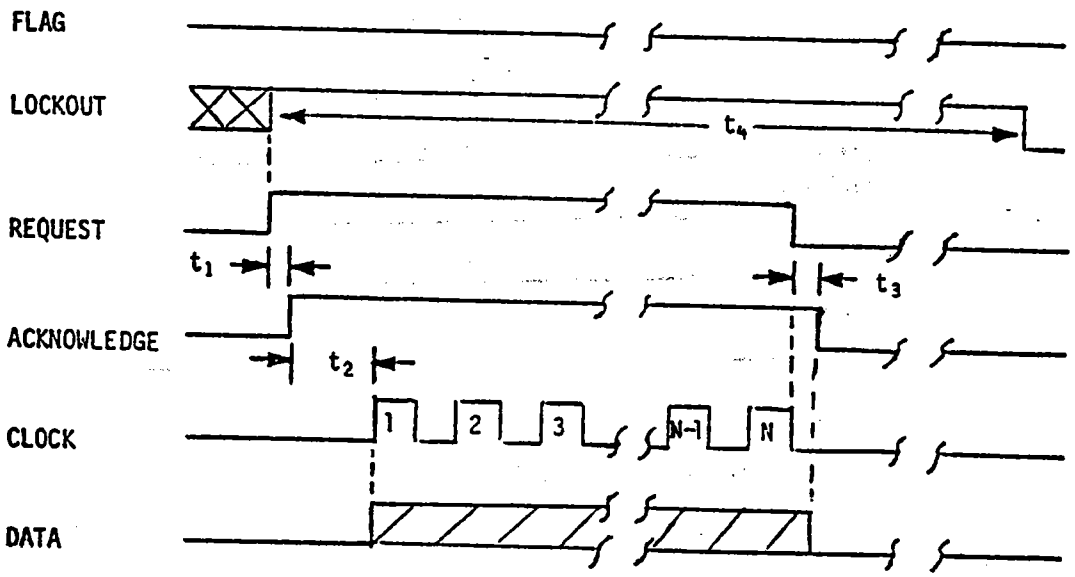


FIGURE 9: Serial Digital Interface



NOTE: (1) N equals 17 times the number of words
(2) t_1 and t_3 are less than 200 nanoseconds
(3) t_2 is less than 500 nanoseconds
(4) t_4 is design dependent

Figure 12. Serial Digital Input Interface Timing Diagram for Terminal Initiation of Transfer

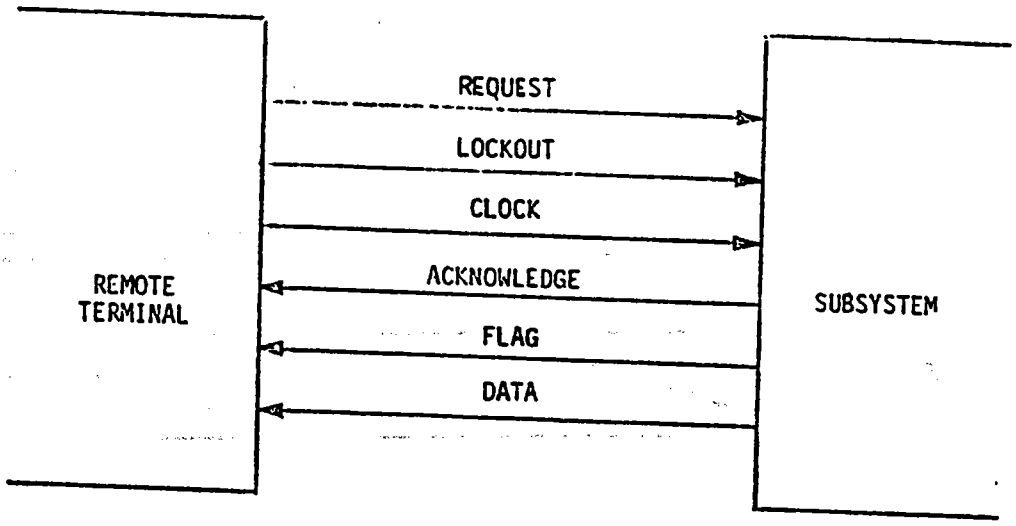


Figure 10. Serial Digital Input Interface

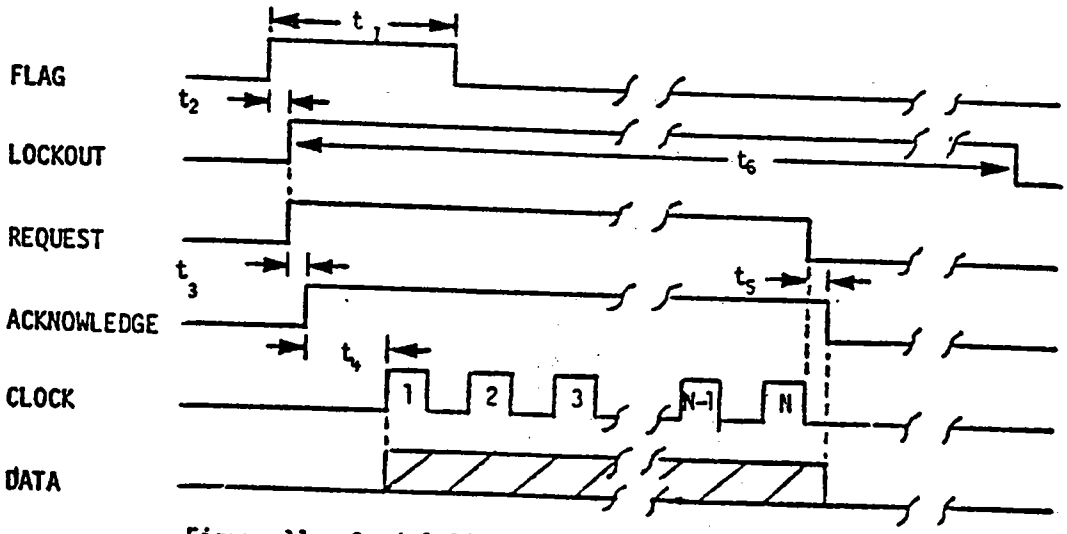


Figure 11. Serial Digital Input Interface Timing Diagram for External Initiation of Transfer

NOTE: (1) N equals 17 times the number of words
(2) t_1 is less than 10 and greater than 1 microsecond
(3) t_2, t_3 and t_5 are less than 200 nanoseconds
(4) t_4 is less than 500 nanoseconds
(5) t_6 is design dependent

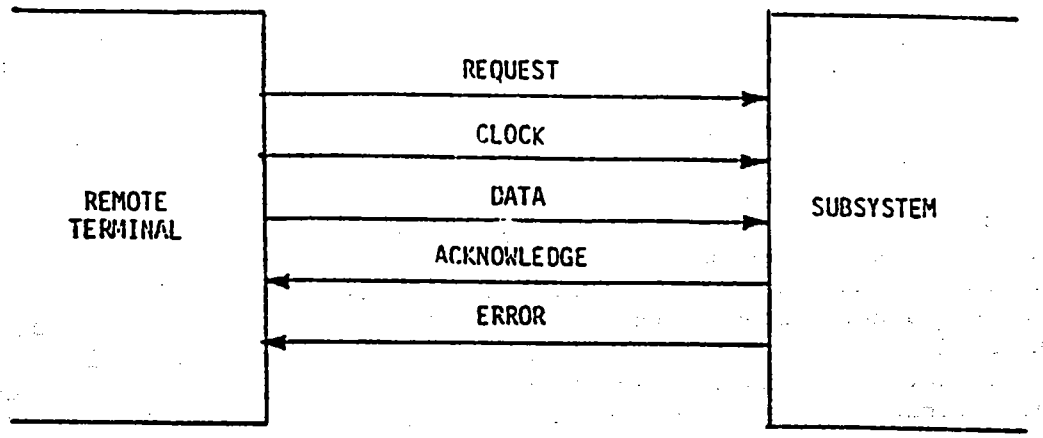
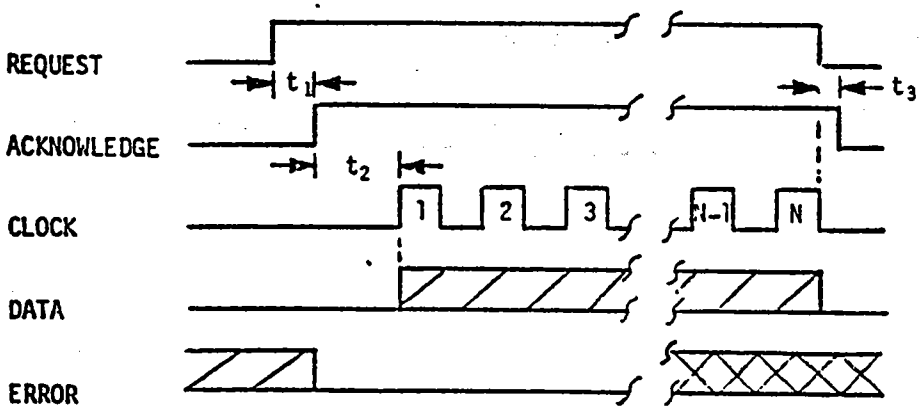


Figure 13. Serial Digital Output Interface



NOTE: (1) N equals 17 times the number of words
(2) ERROR line is based on parity check by subsystem
(3) t_1 and t_3 are less than 200 nanoseconds
(4) t_2 is less than 500 nanoseconds

Figure 14. Serial Digital Output Interface Timing Diagram

4.4.1.2 Serial digital output. A serial digital output interface is a set of five signals between an external device and the remote terminal. This interface is shown in figure 13. The functions of each of these five signals is defined in table I. The timing diagram for the data output sequence using these five signals is shown in figure 14. The performance of a data output sequence can be initiated by either of two bus controller actions. The bus controller can send a new data block to the remote terminal, and the receipt of this data block shall initiate a data output sequence. The bus controller can also directly command the remote terminal to begin a data output sequence using the data block that the remote terminal has available. In either case, once a data output sequence is initiated, the serial interface shall always transfer the complete set of data, and when the data transfer is complete the remote terminal shall examine the ERROR line.

4.4.1.3 Signal characteristics. The characteristics of serial digital signals shall be in accordance with the following:

a.	Data code	Non-return-to zero (NRZ)
b.	Type	Differential and balanced
c.	Data word	16 bits followed by one bit of odd parity
d.	Data rate	One megabit plus or minus 10 percent
e.	Rise and fall time	As specified in 4.2.5.3.2
f.	Output voltage	Zero: -0.5 to 0.5 volts One: 2.4 to 5.5 volts
g.	Common mode output voltage	The common mode output voltage (measured from each line to the signal common) of the output circuit shall be no greater than plus or minus 0.5 volt peak
h.	Short and Over-voltage protection	The output circuit shall not be damaged when subjected to shorts to ground or a voltage of plus or minus 20 volts
i.	Message size	A fixed number of words for each request with a maximum of 32 words
j.	Bit priority	As specified in 4.2.2.

4.4.2 Discrete signals. The discrete interface shall be double-ended, and shall employ the following logic levels:

Zero:	-0.5 to 0.5 volts
One:	2.4 to 5.5 volts

The input circuits shall present a minimum impedance of 10K ohms. Overvoltage faults to an input of up to plus or minus 20 volts shall not damage the input. The output circuits shall be capable of providing a minimum output current of 100 milliamperes. Short circuits on either inputs or outputs shall not damage the circuits.

4.5 Bus controller. The controller shall be responsible for sending data bus commands, participating in data transfer, receiving status response and monitoring system status as defined in this standard. The controller may be embodied as either a stand alone hardware unit whose sole function is to control the data bus(s), or contained within the I/O section of an airborne computer. The controller shall be programmable and shall operate under software (or firmware) control. Individual application requirements shall determine the choice as to which form of controller is used.

Custodian:
Air Force - 11
Navy - AS
Army -

Preparing activity:
Air Force - 11

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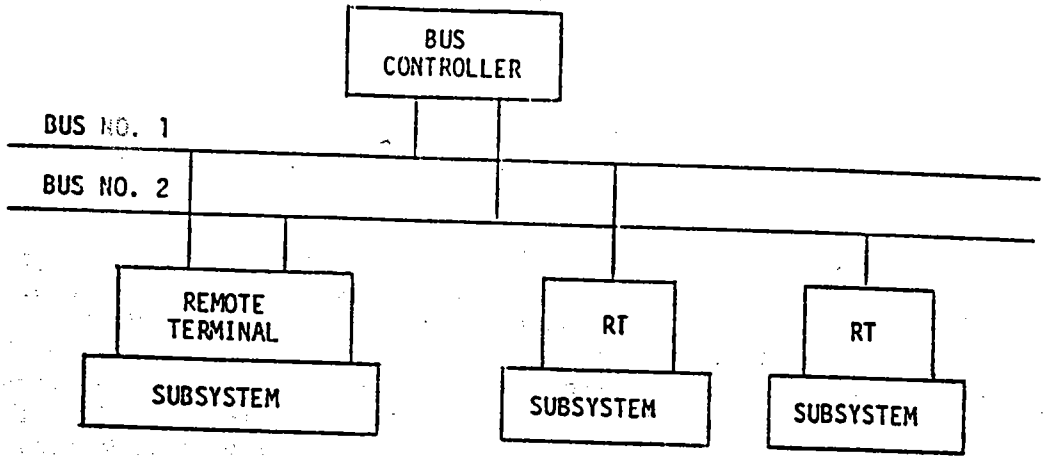

FIGURE 10.1

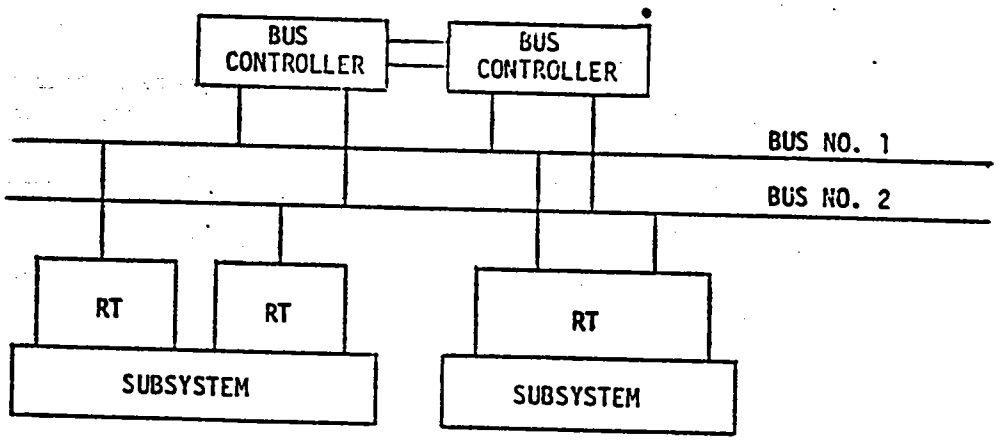

FIGURE 10.2

NOTE: RT - Remote Terminal

ILLUSTRATIONS OF POSSIBLE REDUNDANCY

APPENDIX

10. General. The following paragraphs in this appendix are presented in order to discuss certain aspects of the standard in a general sense. They are intended to provide a user of the standard more insight into the aspects discussed.

10.1 Redundancy. It is intended that this standard be used to support rather than to supplant the system design process. For this reason, the standard is deliberately vague concerning the use of redundancy in implementing a multiplex data bus system. The system designer should utilize this standard as the needs of a particular application dictate. The use of redundancy, the degree to which it is implemented, and the form which it takes must be determined on an individual application basis. Figures 10.1 and 10.2 illustrate some possible approaches to dual redundancy. These illustrations are not intended to be inclusive, but rather representative. It should be noted that analogous approaches exist for the triple and quad redundant cases.

10.2 Bus controller. The bus controller is a key part of the data bus system. The functions of the controller, in addition to the issuance of commands, must include the constant monitoring of the data bus and the traffic on the bus. It is envisioned that most of the routine minute details of bus monitoring (e.g., parity checking, terminal non-response time-out, etc.) will be embodied in hardware, while the algorithms for bus control and decision making will reside in software. It is also envisioned that, in general, the bus controller will be a general purpose airborne computer with a special input/output (I/O) unit to interface with the data bus. In the case of a large aircraft, such as a bomber, the multiplex bus control problem may be of sufficient complexity to warrant the employment of a dedicated bus controller. While in a smaller, fighter-type aircraft, the control function will probably be incorporated into a computer which is also utilized for the navigation and weapon delivery functions. It is important to remember that the controller will be the focal point for modification and growth within the multiplex system, and thus the software must be written in such a manner as to permit modification with relative ease.